chemical vapor deposition to form a layer of gate material; and

etching the gate material to a desired pattern using a reactive ion etch process.

30.(Amended) The method of claim [21,] 29 wherein etching the gate material further [includes] comprises using plasma etching in combination with the reactive ion [etching] etch process.

31.(Amended) The method of claim [21] 29, further comprising conductively doping the [gate material prior to] silicon carbide compound $Si_{1-x}C_x$ while depositing the [gate material] silicon carbide compound $Si_{1-x}C_x$ on the insulating layer.

32.(Amended) The method of claim [21] 29, further comprising oxidizing the gate material to form a thin layer of oxide on the gate material.

33.(Amended) The method of claim 21[,] wherein the gate [is] comprises a floating gate, and further comprising:

forming [a second insulating layer] an intergate dielectric over the floating gate; and

forming a polysilicon control gate over the [second insulating layer] intergate dielectric.

Please add the following new claims:

36.(New) The method of claim 21 wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on the channel region by dry thermal oxidation.

37.(New) The method of claim 21 wherein forming a source region comprises forming a p-type source region and a p-type drain region in an n-type silicon substrate, a channel region being between the p-type source region and the p-type drain region.

38.(New) The method of claim 21 wherein forming a source region comprises forming an n-type source region and an n-type drain region in a p-type silicon substrate, a channel region being between the n-type source region and the n-type drain region.

39.(New) The method of claim 21 wherein forming a gate further comprises doping the gate by ion implantation.

40.(New) The method of claim 21 wherein forming a gate further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

41.(New) The method of claim 40 wherein depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer further comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer.

42.(New) The method of claim 21, further comprising:

forming a well region in the semiconductor substrate;

forming field oxide on the semiconductor substrate to define an active region;

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

43.(New) A method of fabricating a transistor comprising:

forming an insulating layer on a substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the substrate.

44.(New) The method of claim 43 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor

deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

45.(New) The method of claim 43, further comprising:

selecting x to establish an approximate barrier energy between the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer;

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

46.(New) The method of claim 43, further comprising:

forming a source region and a drain region in the substrate and separated by a channel region in the substrate;

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

47.(New) The method of claim 43, further comprising:

forming a source region and a drain region in the substrate and separated by a channel region in the substrate;

oxidizing the gate by plasma oxidation to form an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

48.(New) The method of claim 43, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant.

49.(New) The method of claim 43, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation.

50.(New) A method of fabricating a transistor comprising:

forming an insulating layer on a silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation; and

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the substrate.

51.(New) The method of claim 50 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

52.(New) The method of claim 50, further comprising:

selecting x to establish an approximate barrier energy between the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer;

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

doping the layer comprises doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

53.(New) The method of claim 50, further comprising:

forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate;

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

54.(New) The method of claim 50, further comprising:

forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate;

oxidizing the gate by plasma oxidation to form an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

55.(New) A method of fabricating a transistor comprising:

forming an insulating layer on a silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation;

and

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the substrate.

56.(New) The method of claim 55 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

57.(New) The method of claim 55, further comprising:

selecting x to establish an approximate barrier energy between the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer;

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

58.(New) The method of claim 55, further comprising:

forming a source region and a drain region in the silicon substrate and separated by a

channel region in the silicon substrate;

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

59.(New) The method of claim 55, further comprising:

forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate;

oxidizing the gate by plasma oxidation to form an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

60.(New) A method of fabricating a floating gate transistor comprising:

forming an insulating layer on a substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric.

61.(New) The method of claim 60 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

62.(New) The method of claim 60, further comprising:

selecting x to establish an approximate barrier energy between the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer;

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

forming a source region and a drain region in the substrate and separated by a channel region in the substrate; and

wherein forming an insulating layer comprises forming a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.

63.(New) The method of claim 60, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant.

64.(New) The method of claim 60, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation.

65.(New) A method of fabricating a floating gate transistor comprising:

forming an insulating layer on a silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the silicon substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric.

66.(New) The method of claim 65 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

67.(New) The method of claim 65, further comprising:

selecting x to establish an approximate barrier energy between the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer;

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate; and

wherein forming an insulating layer comprises forming a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.

68.(New) A method of fabricating a memory cell comprising:

forming an insulating layer on a substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric.

69.(New) The method of claim 68 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

70.(New) The method of claim 68, further comprising:

selecting x to establish an approximate barrier energy between the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer;

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

forming a source region and a drain region in the substrate and separated by a channel region in the substrate; and

wherein forming an insulating layer comprises forming a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the

insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.

71.(New) The method of claim 68, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant.

72.(New) The method of claim 68, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation.

73.(New) A method of fabricating a memory cell comprising:

forming an insulating layer on a silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the silicon substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric.

74.(New) The method of claim 73 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC

plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

75.(New) The method of claim 73, further comprising:

selecting x to establish an approximate barrier energy between the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer;

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate; and

wherein forming an insulating layer comprises forming a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.